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CONFIGURABLE 8 PORTS DETERMINISTIC ETHERNET SWITCH

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ABSTRACT

The Word Avionics is the mix of the Aviation and electronics, which could be characterized as hardware of air crafts, artificial satellites and spacecrafts.MIL-1553 as its communication protocol for Avionics networks. But, MIL-1553 communication is half duplex, asynchronous and works at 1Mbps which will be unable to oblige the future communication execution necessities of bandwidth and practicality. So a need exists to enhance bandwidth, dependability and maintainability.so the new system is built up where it manages the communication between the different avionic PC frameworks. The data from one Avionic computer system to another avionic computer system is established in an AFDX arrange through the AFDX Ethernet switches. Avionics Full Duplex Switched Ethernet (AFDX) is a standard that portrays the electrical and protocol particulars (IEEE 802.3 and ARINC 664, Part 7) for the trading of information between Avionics Subsystems. In addition to providing higher speed information exchange, the switches are configurable. The switch is to be executed in FPGA ZYNQ in the hardware design tool XILINX VIVADO. The last stage incorporates testing the switch within the sight of different Avionic PC frameworks and acquiring a conclusion in regards to applications.

KEYWORDS: ARINC 664P7, MIL-1553, ZYNQ FPGA, AFDX

I. INTRODUCTION

Avionics Full-Duplex Switched Ethernet Network (AFDX), initially The Word "Avionics" is the combination of the Aviation and electronics, which could be characterized as hardware of aircrafts, manufactured satellites and space crafts The Scientist Mr.Collinson notices that the term avionics "was first utilized as a part of the United State of America (USA) in the early 1950s and has since gained wide scale usage and acceptance" simply it is Avionics Full-Duplex Ethernet network protocol.

Previously MIL-1553 was used for avionic papers. But, MIL-1553 communication is half duplex, asynchronous and works at 1Mbps which will most likely be unable to take into account the future communication execution prerequisites of bandwidth and maintainability. So a need exists to enhance bandwidth, reliability and maintainability while in the meantime diminishing the physical measurements of size, weight and number of connectors. Another system foundation is expected to give greater adaptability in avionics system design and adapt to the expanding number of interconnections between systems.

The proposed paper is usage of 8/16/24 - port AFDX switch on ZYNQ FPGA and furthermore to shape a deterministic system implies that all the AFDX End systems associated through AFDX switches by means of Virtual connections, finally the uses information speed is 100Mbps full-duplex switched Ethernet as indicated by ARINC-664Part7.

Benefits of this paper is repetition can be accomplished i.e. there is no reiteration of frames at yield of end-system and another is complexity of the system can be diminished. The paper is composed as takes after. AFDX protocol is given in segment II. Section III gives AFDX diagram, while Section IV manages past strategies. Section V manages proposed paper lastly Section VI manages simulation results and end test setup results and Section VII finishes up the paper and gives rules to future degree.

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II. PROPOSED TECHNIQUE

The proposed paper is usage of 8 - port AFDX switch on ZYNQ FPGA and to form a deterministic system implies that all the AFDX End systems associated through AFDX switches by means of Virtual links, it uses the information speed is 100Mbps full-duplex switched Ethernet as indicated by ARINC-664P7 protocol. Fundamental advantages of this paper is redundancy can be accomplished i.e. there is no reiteration of frames at output of end-system and another is intricacy of the system can be diminished. The tools are utilized - for synthesis Xilinx Vivado 2014.4 and xilinx 14.6 ISE test system and the packet flow at end-system can be caught by Wire-shark programming. The proposed engineering of 8X8 AFDX switch as appeared beneath figure

Figure 1: proposed architecture of 8X8 AFDX switch

III. AFDX PROTOCOL

AFDX Protocol Aircraft Data Networks (ADN) principally uses the ARINC 429 standard. This standard, created more than thirty years back and still broadly utilized today, has ended up being profoundly solid in wellbeing basic applications. ARINC 429 systems, which can be found on an assortment of aircraft from both Boeing and Airbus organizations, use a unidirectional transport with a single transmitter and up to twenty receivers. An information word comprises of 32 bits conveyed over a twisted cable link. There are two rates of transmission: fast works at 100 Kbit/s and low speed works at 12.5 Kbit/s. Another standard, ARINC 629, presented by Boeing for the 777 aircraft gives expanded information velocities of up to 2 Mbit/s and permitting a greatest of 120 information terminals. ARINC 629 system works without the utilization of a transport controller, subsequently expanding the reliability of the system engineering.

One of the essential downside of this system sort is that it is certain to common aircraft applications, requiring custom hardware which can include noteworthy cost and improvement time to the flying machine. ARINC664 Part7 is characterized as the next generation aircraft data network (AFDX). It depends on IEEE 802.3 Ethernet, empowering more prominent potential utilization of Commercial Off-The-Shelf (COTS) hardware, along these lines diminishing aircraft cost and improvement time. AFDX was created via Airbus Industries for the A380, has since been acknowledged by Boeing and utilized on the Boeing 787 Dream liner, and is being utilized or considered today for different applications

IV. AFDX OVERVIEW

In this area manages about outline of AFDX and switch description and end system detail, and virtual link idea and furthermore the concise clarification of Jitter and Bag concept etc. Primarily AFDX network comprises of three sections

- AFDX Switch
- AFDX End system
- AFDX Virtual links

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An aircraft data arrange has been portrayed elsewhere in this standard as a profiled type of an IEEE 802.3 Ethernet utilizing IP addressing and related transport protocols. ARINC664 Part7 depicts a subset of this network, where nature of organization including helpful movement is essential. The AFDX network is a one of a kind occurrence of a profiled network. A deterministic network may talk with a broader profiled network and by acceptance, with a reliable network through switches or entryways.Figure2 depicts this network progression.

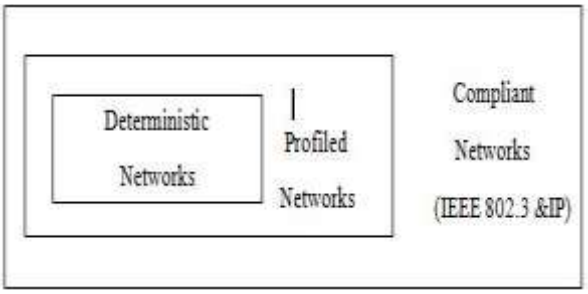

Figure 2: AFDX Network Hierarchy

A. AFDX Switch

The AFDX switch comprises of five practical blocks that cooperate with each other, as appeared in figure.

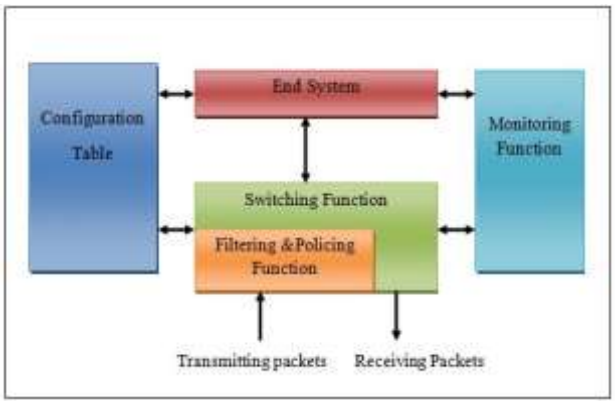

Figure 3: Functional elements of AFDX Switch

All frames arrive at the switch in the Filtering and policing function arranges where they are separated in different advances. That applies administers about frame integrity, frame length, traffic budget and satisfactory goal. The core of the switching action is performed by the switching function. Frames separated by the filtering and policing function are sent to the fitting physical yield ports where they leave the switch once more.

The most important functions are controlled by configuration information contained in static configuration tables. The end framework organizes gives the way to communicate with the switch (gets frames devoted to the switch and enables the switch to send frames). This is utilized for information stacking and monitoring functions. All operations are observed by monitoring functions that logs events, for example, the entry of a frame or a failed CRC check and moreover makes measurements about the inward circumstance. Since the switch is a piece of a network, it speaks with the network administration function for operational data and for health related data. The frame size value appeared in figure.

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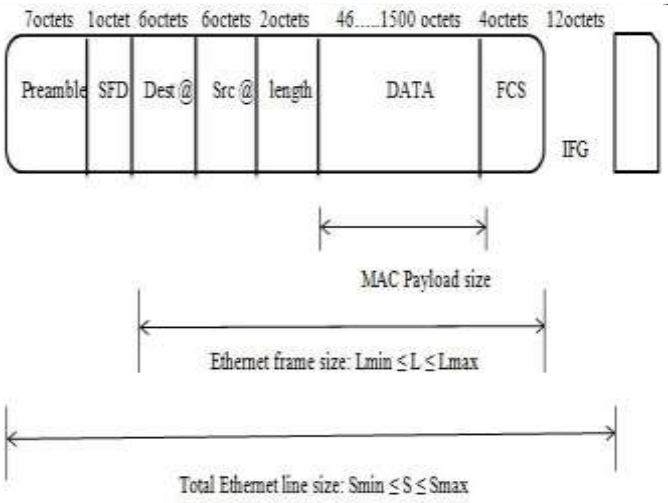

Figure 4: Frame size values

The actual time a frame occupies the Ethernet line (s). Therefore, all fields have to be taken into account: IFG (12 octets) + Preamble (7 octets) + SFD (1 octet) + MAC Frame size (L = 64 to 1518 octets).

Filtering function

The filtering makes the switch disperse just substantial frames to choose destinations. Upon entry in a switch, each frame is analyzed and the substance of specific fields of the frame header (e.g. destination address field, frame check arrangement field, and so forth.) and the development of the frame itself is observed:

- The frame size: whether the frame is either longer or shorter than the envelope allows.
- The frame integrity: whether the FCS embedded in the frame matches the calculation upon reception.
- The frame path: whether the destination requested by the content of the Destination Address field (which in case of the AFDX is the Virtual Link Identifier) of the arriving frame is permitted or not.

On the off chance that the frame properties don't conform to the configuration parameters, the frame is separated i.e. disposed of, and at least one MIB sections refreshed. The meaning of the MIB passages and additionally the refresh conditions and procedures are determined in the significant determination archive.

The following aspects of the frame are tested as part of the filtering function:

1) Destination address validity (Ethernet Address corresponds to a valid VL, including constant field)
2) This VL is valid to be received on that destination port (according to the switch configuration table)
3) Frame Check Sequence validity
4) Ethernet frame size (L) is an integral number of octets(alignment)
5) Ethernet frame size (L) in the range [64 octets, 1518 octets]
6) Ethernet frame size (L) less than or equal to Lmax 7)Ethernet frame size (S) greater than or equal to Smin, only in case where byte-based traffic policing is used

Traffic policing

This segment portrays a model of an algorithm that performs traffic based policing on the Destination Address premise. The Destination Address field contains the data that is utilized to recognize a Virtual Link in an AFDX domain. A Virtual Link characterizes a traffic flow that has certain properties, for example, a group of recipients, or a base allowed gap between two frames. This traffic flow must be kept up segregated to ensure its related properties. So as to use with regards to this determination an indistinguishable wording from the one utilized as a part of business reports the Destination Address is utilized synonymously with the term Virtual Link or "VL."

The jitter phenomenon is reliant upon Virtual Link and switch attributes, as it is a component of the traffic of the aggregate of every Virtual Link landing at a specific switch. In the event that a Virtual Link traverses a few switches, the genuine jitter might be diverse on each of the transitional switch. Be that as it may, greatest esteems for latency and jitter for any switch give an upper bound.

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The traffic-policing model is portrayed from an End-System perspective since End-Systems are the principle traffic generators into the switch, appeared in Figure 5. Display based depiction of the switch gives a switch driven perspective of the properties anticipated from a legitimate usage of the switch. The switch may execute one of the two algorithm, either Byte-based or Frame based, or them two. The decision of the algorithm will affect the strategy used to demonstrate the schedulability of the system.

The Switch ought to have a traffic prioritization system based on MAC destination address with 2 traffic classes: High Priority and Low Priority. The need level ought to be characterized in the configuration table on a Virtual Link basis.

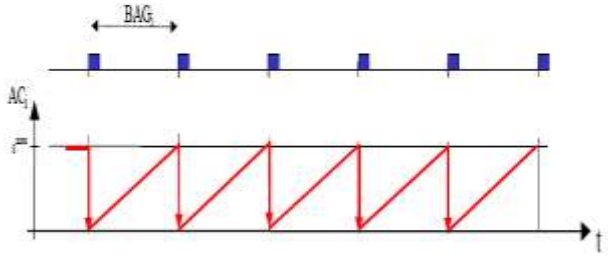

Figure 5: Example of Traffic without Jitter

Description of the policing algorithm: Initially, the ACcount for VLi (also called ACi, expressed in bytes) is set to

Simax (1+Ji/BAGi)

- ACi is checked every time a frame of VLi arrives in the switch.
- Let s be the total Ethernet line size of the received frame (S = Ethernet frame size (L) + 20 octets; the 20 octets correspond to IFG+Preamble+SFD).

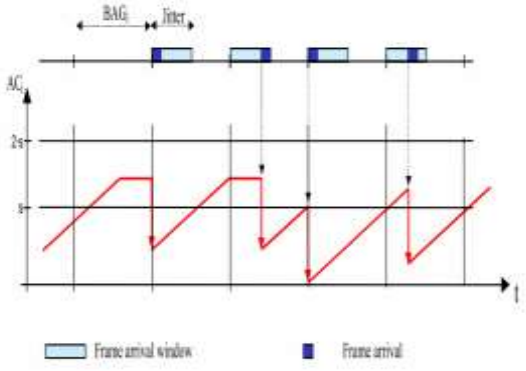

Figure 6: Example of Traffic with Jitter = BAG/2

A traffic policing mechanism ought to be executed on the switch keeping in mind the end goal to ensure fault control capacity of the system. Since a fizzled End System must not aggravate the system, any frame having a place with a traffic stream that isn't agreeable with the system configuration ought to be disposed of. The Configuration table has a connection between MAC destination address, ACi, BAG, Jitter, Smax, and in the end Smin for the situation where byte-based traffic policing is utilized. Traffic policing ought to be based on parameters: BAG, Jitter, Smax, and in the long run Smin for the situation where byte-based traffic policing is utilized. For each VL or gathering of VLs having a similar record, the Traffic Policing capacity ought to approve one BAG an incentive as per the configuration table.

The Traffic Policing capacity of the switch ought to at any rate be configurable for BAG values in the range 1ms to 128 ms. For each VL or gathering of VLs having a similar account, the Traffic Policing capacity ought to approve one most extreme Jitter value, as indicated by the configuration table. The traffic policing capacity

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ought to at least be configurable for most extreme permitted Jitter values in the range 0 to 10 milliseconds. This infers ACi has a most extreme size of at any rate:

$$ACimax. = Simax (1+Ji/BAGi)$$

The traffic policing function should be able to handle at least Ethernet frames sizes (L) in the range [64-1518] octets.

B. End System

The fundamental function of the End System (ES) is to give services, which ensure a safe and solid information trade to the parcel programming. Quality of Service (QoS) gives a technique to sorting traffic and for guaranteeing that specific classifications of traffic will dependably stream over the system at the service level to which they are entitled, paying little heed to contending requests.

C. Virtual Link

Portrayal of the "Virtual Link" idea is displayed in Figure 6, since it is generally utilized as a part of this undertaking. An end system might be designed to just get VLs and not transmit VLs, or the opposite; consequently, an ES can start or get zero VLs. End-systems trade Ethernet frames through VL. Just a single End System inside the Avionics system ought to be the source of any one VL. A Virtual Link is a theoretical communication protest, which has the accompanying properties:

A Virtual Link defines a logical unidirectional connection from one source end-system to one or more destination end-systems, shown in Figure 7.

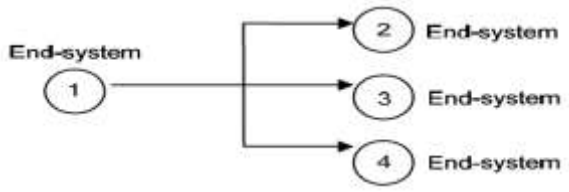

Figure 7: virtual link path

Each Virtual Link has a devoted most extreme bandwidth. This bandwidth is distributed by the System Integrator. The ES ought to give logical isolation regard to accessible bandwidth among the Virtual Link it supports. Notwithstanding the endeavored use of a VL by one parcel, the accessible Bandwidth on some other VL is unaffected. For each Virtual Link, the End System ought to keep up the requesting of information as delivered by a segment, for both transmission and reception (ordinal integrity).

D. Scheduling

In a transmitting end system with numerous VLs, the scheduler multiplexes the Different flows originating from the controllers, as outlined in figure 8,it shows how unregulated flow of packets changed over in to uniform flow.

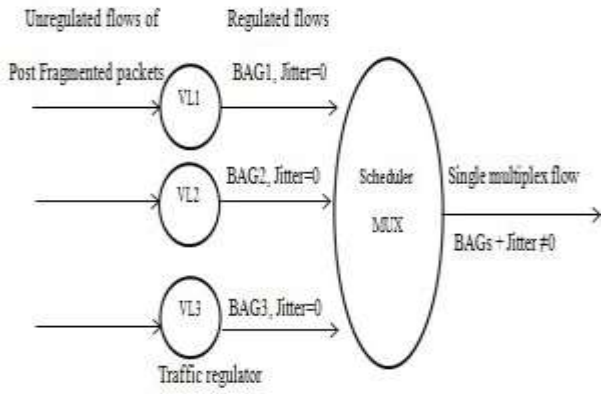

Figure 8: Model of the Scheduled Flow Control Mechanism

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At the output of the scheduler, for a given Virtual Link, frames can show up in proliferated time interval. This interval is characterized as the most extreme permissible jitter. This jitter is presented by the scheduler.

E. **Jitter**

Jitter is variation of packet landing time after bag. In transmission, the most extreme permitted jitter on each VL at the output of the end system ought to agree to both of the accompanying formula.

$$\begin{cases} max\_jitter \le 40\mu s + \dfrac{\sum_{i \in \{set\ of\ VLs\}} \left(20\ bytes + L^{max}{}_{bytes}\right) \times 8\ Bits/bytes}{Nbw_{\ bits/s}} \\ max\_jitter \le 500\mu s \end{cases}$$

MAC Destination Address

A Virtual Link should just be distinguished by the MAC destination address as represented in Figure 9, and the MAC source address of AFDX frames ought to be the MAC unicast address used to recognize the physical Ethernet interface. A MAC destination address in the AFDX frame ought to be a Group and Locally Administered address and ought to be consistent with the accompanying format.

48 bits	
Constant field 32 bits	virtual link identifier 16 bits
XXXX XX11 XXXX XXXX XXXX XXXX XXXX XXXX	

Figure 9: MAC Multicast Addressing Format

Every ES ought to get "constant field" and "Virtual Link Identifier" values from the system integrator. The values are not indicated in ARINC Specification 664. The constant field ought to be the same for every ES in any given AFDX arrange. The least significant bit of the first byte shows the group address (always = 1). With a specific end goal to utilize the standard Ethernet frame, MAC group addresses ought to be utilized to send frames from End System to End System(s). The second to least significant bit of the primary byte demonstrates the privately regulated address (always = 1).

MAC Source Address

The MAC Source address ought to be an Individual and Locally Administered address agreeable with IEEE 802.3. The structure of the address is determined in the accompanying format as appeared in figure 10.

Ethernet MAC Controller Identification (48 bits)			
Constant field 24- Bits	User_Defined_ID 16 - bits	Interface_ID 3- bits	Constant field 5- bits
"0000 0010 0000 0000 0000 0000"	"nnnn nnnn nnnn nnnn"	"mmm"	"0 0000"

Figure 10: MAC Source Addressing Format

F. Redundancy Management

The Redundancy Management (RM) accepts that the system is working appropriately and, specifically, the deterministic properties are confirmed. As appeared in figure11 Definitions:

- Redundant VL implies that similar frames are sent through both system, A and B.
- Non-redundant VL implies that (potentially unique) frames are sent through either arrange A or B

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On a per VL basis, the ES should be able to receive:

- A redundant VL and deliver to the partition one of the redundant information (RM active).
- A redundant VL and deliver to the partition both redundant information (RM not active).
- A non-redundant VL on either interface and submit information from it to the partition (for this situation, RM can be active or not).

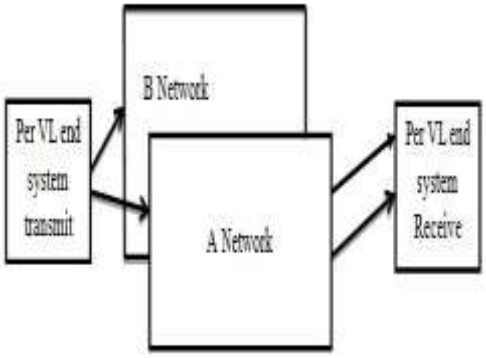

Figure 11: Network Redundancy Concept

V. PREVIOUS TECHNIQUES

MIL-1553 is a communication protocol for its activities. But, MIL-1553 communication is half duplex, asynchronous and works at 1 Mbps which will be unable to take into account the future communication execution necessities of bandwidth and maintainability and delay additionally more. So a need exists to enhance bandwidth, reliability and maintainability while in the meantime decreasing the physical measurements of size, weight and number of connectors. Another system framework is expected to give greater adaptability in avionics system design and adapt to the expanding number of interconnections between systems.

S no	Parameter	Previous Technique	Proposed technique using AFDX 664 P7
1	Redundancy	Not achieved	Redundancy achieved without errors.
2	Complexity	more	Reduced because here using virtual links
3	Data speed	1Mbps	100 Mbps achieved
4	Network	Deterministic	Deterministic and profiled
5	Frame Length	It not suitable for maximum frame length	Here we consider [64, 1518] means Lmin=64bytes and Lmax=1518 bytes.
6	Bandwidth	More	Link B.W= Lmax/BAG. Here B.W reduced.
7	Type of Data	Half duplex	Full duplex

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VI. CONCLUSION

ARINC 664/AFDX (Avionics Full Duplex Switched Ethernet) protocol is being used as the back bone for all systems including flight controls, cockpit avionics, air-conditioning, power utilities, fuel systems, landing gear and other. Simply it mainly used in COTS, and high speed commercial Ethernet with provisions for guaranteed deterministic timing and redundancy required for avionics applications. The RTL for the proposed 8 port AFDX switch architecture was designed and simulated with certain predefined test cases for 8-port Switch. A Configuration Table having 16 entries was given based on which the traffic was filtered and policed. The behavioral simulation was found to work as desired, thereby verifying the functionality of the design and also functionality was tested by ZYNQ FPGA, by using AFDX test setup means End systems are communicate with AFDX switch via virtual links then observing data speed with 100Mbps [10] and redundancy also achieved, packet flow can be observed by Wire shark software and whole complexity of network reduced finally formed the deterministic network.

VII. FUTURE SCOPE

This paper is extendable to more ports of AFDX switch and also it can implement on other FPGA boards for best example net FPGA and this AFDX protocol helpful in high speed Ethernet network applications it will extendable to data speed is 1Gbits/sec..

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